IN THE CLAIMS

The following is a complete listing of the claims:

1.(Original) A semiconductor device, comprising:

a plurality of boundary scan cells; and

a demultiplexer; wherein the semiconductor device includes a first configuration wherein a primary boundary scan chain is formed using the plurality of boundary scan cells and a first output of the demultiplexer, and wherein the semiconductor device includes a second configuration wherein a secondary boundary scan chain is formed using the plurality of boundary scan cells, a plurality of boundary scan cells in at least one external device and a second output of the demultiplexer.

2. (Original) The semiconductor device of claim 1 wherein the semiconductor device is a programmable power sequence controller.

3. (Original) The semiconductor device of claim 1, further comprising a configuration memory cell, wherein the state of the configuration memory cell controls whether the semiconductor device is in the first configuration or the second configuration.

4. (Original) The semiconductor device of claim 1, further comprising a JTAG port having a TDI and a TDO pin, wherein the primary boundary scan chain extends from the TDI pin, through the plurality of boundary scan cells in the semiconductor device to the first output of the demultiplexer, and from the first output of the demultiplexer to the TDO pin.

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5. (Original) The semiconductor device of claim 4, further comprising a first I/O pin, wherein the secondary boundary scan chain extends from the TDI pin, through the plurality of

boundary scan cells in the semiconductor device to the second output of the demultiplexer, from the second output of the demultiplexer to the first I/O pin, from the first I/O pin through the plurality of boundary scan cells in the at least one external device .

6. (Original) The semiconductor device of claim 5, wherein the first output of the demultiplexer couples to the TDO pin through a tri-state buffer.

7. (Original) The semiconductor device of claim 5, further comprising a second I/O pin, wherein the secondary boundary scan chain extends from the plurality of boundary scan cells in the at least one external device through the second I/O pin to the TDO pin.

8. (Original) The semiconductor device of claim 7, further comprising a multiplexer having an output coupled to the TDO pin, the multiplexer having a first input coupled to the second I/O pin and a second input coupled to the first output of the demultiplexer, wherein in the first configuration, the multiplexer is configured to select for the second input, and wherein in the second configuration, the multiplexer is configured to select for the first input.

9. (Original) The semiconductor device of claim 8, wherein the output of the multiplexer couples to the TDO pin through a tri-state buffer.

10. (Original) The semiconductor device of claim 1, wherein the at least one external device comprises a plurality of external devices, and wherein the semiconductor device comprises a programmable sequencer operable to control the power sequencing of the plurality of external devices.

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11. (Original) A method, comprising:

providing a semiconductor device including a first plurality of boundary scan cells forming a shift register, a demultiplexer receiving the output of the shift register, a TDO

pin, and a first I/O pin, and providing at least one external device having a second plurality of boundary scan cells;

configuring the demultiplexer into a first configuration to couple the output of the shift register to the TDO pin such that a primary boundary scan chain is formed in just the first plurality of boundary scan cells; and

configuring the demultiplexer into a second configuration to couple the output of the shift register to the first I/O pin, such that a secondary boundary scan chain is formed including both the first and the second plurality of boundary scan cells.

12. (original) The method of claim 11, further comprising:

providing a second I/O pin and a multiplexer for the semiconductor device, the multiplexer having a first input coupled to an output of the demultiplexer and having a second input coupled to the second I/O pin;

when the demultiplexer is in the first configuration, configuring the multiplexer to couple its first input to the TDO pin; and

when the demultiplexer is in the second configuration, configuring the multiplexer to couple its second input to the TDO pin.

13. (Original) A device, wherein the device is configurable to form a secondary boundary scan chain with a first plurality of boundary scan cells within at least one external device, comprising:

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a second plurality of boundary scan cells;

a TDI pin;

a TDO pin; and

means for forming a primary boundary scan chain between the TDI pin and the TDO pin including only the second plurality of boundary scan cells and for forming a secondary boundary scan chain between the TDI pin and the TDO pin including the first and the second plurality of boundary scan cells.

14. (Original) The device of claim 13, wherein the means includes a configuration memory cell, the state of the configuration memory cell controlling whether the primary or the secondary boundary scan chain is formed.

15. (Original) The device of claim 14, wherein the means includes a demultiplexer controlled by the state of the configuration memory cell.

16. (Original) The device of claim 15, wherein the means forms the secondary boundary scan chain using a first I/O pin.

17. (Original) The device of claim 16, wherein the means further forms the secondary boundary scan chain using a second I/O pin.

18. (Original) A semiconductor device, comprising:

a data input pin adapted to receive configuration and/or test data;

first and second data output pins adapted to transmit configuration and/or test data; and

a plurality of scan cells forming a scan chain,

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wherein the semiconductor device is configurable to couple the scan chain between the data input pin and the first data output pin in a first configuration and to couple the scan chain between the data input pin and the second data output pin in a second configuration.

19. (Original) The semiconductor device of claim 18 wherein the semiconductor device includes a JTAG port, the data input pin being a TDI pin and one of the data output pins being TDO pins.

20. (Original) The semiconductor device of claim 18, wherein the semiconductor device is a programmable logic device.

21. (Original) The semiconductor device of claim 18, wherein the semiconductor device is a programmable power supply sequence controller.

22. (Original) The semiconductor device of claim 18 including a second data input pin adapted to receive configuration and/or test data from a second device, the second data input pin coupled to the first data output pin with the semiconductor device in the second configuration.

23. (Original) The semiconductor device of claim 18, wherein the semiconductor device is a first logic device, and the second data output pin of the first logic device is coupled to a data input pin of a second logic device, the first logic device forming a first scan chain in the first configuration and the first and second logic devices forming a second scan chain in the second configuration.

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24. (Original) The logic device of claim 23, wherein the first logic device includes a second data input pin coupled to a data output pin of the second logic device, the second data input

pin adapted to receive configuration and/or test data from the second logic device in the second configuration.

25. (Original) A method of programming and/or testing semiconductor devices using scan chains, the method comprising:

powering up a first semiconductor device;

configuring the first semiconductor device to create a first scan chain that excludes a second semiconductor device that has not yet been powered up;

programming and/or testing the first semiconductor device using the first scan chain;

powering up the second semiconductor device;

configuring the first semiconductor device to create a second scan chain that includes the first and second semiconductor devices; and

programming and/or testing at least the second semiconductor device using the second scan chain.

26. (Original) The method of claim 25 wherein the first semiconductor device controls the powering up of the second semiconductor device.

27. (Original) The method of claim 25 wherein the acts are executed in the order recited.

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